Please delete the present Abstract of the Disclosure.

Please add the following new Abstract of the Disclosure:

An electrical signal regenerator including an equalizer and a clock data recovery circuit is provided. The clock data recovery circuit is selected when an input signal of a higher bitrate multiplex level is detected, but the clock data recovery circuit is bypassed when an input signal of a lower bitrate multiplex signal is detected. The electrical signal regenerator can be used in an optical switch processing signals of the new OTN according to ITU-T G.709, in which optical signals undergo optical to electrical conversion and are fed to an electrical space switching matrix including a plurality of the switch modules electrically interconnected by means of internal electrical signal paths such as a backplane or electrical cables. The electrical signal regenerator can be coupled to each input of a switching module to check internal cabling of the switching matrix.